ANALOG DEVICES

AN-333
APPLICATION NOTE

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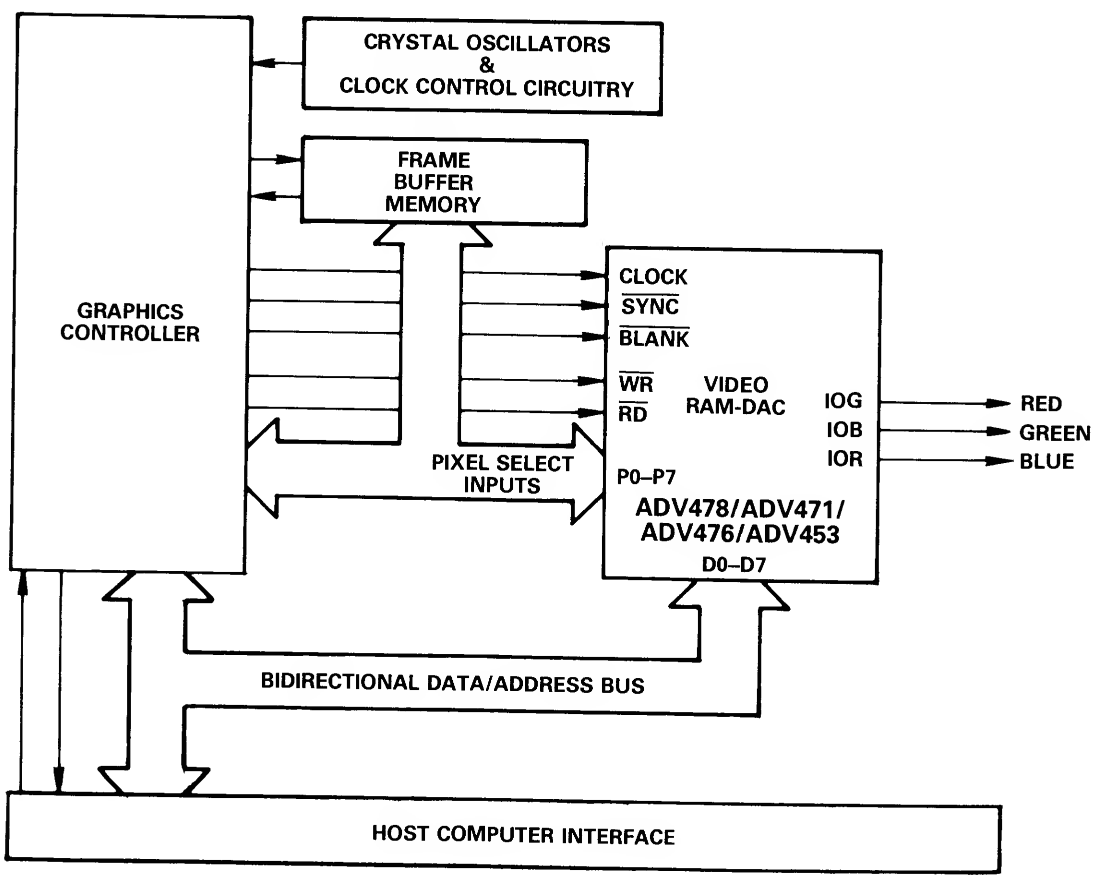
Design and Layout of a Video Graphics System for Reduced EMI

by Bill Slattery and John Wynne

The availability of low cost, high performance video RAM-DACs is a key element in the spread of personal computers into application areas previously considered the preserve of expensive, high-end computer systems. Applications such as Computer Aided Engineering (CAE), Computer Aided Design (CAD), Solids Modelling, Desktop Publishing, etc., are becoming more widespread as the cost of the necessary hardware drops. Successfully incorporating a video RAM-DAC into a personal computer or onto a video graphics plug-in board is not difficult once some basic concepts are grasped and some simple guidelines followed.

This application note is intended as a guide to the design of a video graphics system in terms of Electromagnetic Compatibility (EMC). EMC design will be considered as the technique of reducing radiated emissions and Electromagnetic Interference (EMI) from a high speed video graphics system. EMC implies that the system should not electrically or magnetically interfere with its surroundings, and conversely, the surroundings should not interfere with the operation of the system. In order to provide control of EMI in the radio spectrum, government agencies and other international organizations have established limits relating to EMI, most notably, the U.S. government's FCC Part 15.



Simplified Block Diagram of a Typical Graphics System Using a Video RAM-DAC

OVERVIEW

This application note is divided into a number of sections as outlined below:

1. International EMI Regulatory Bodies – guidelines, testing and radiation limits.
2. System Noise Identification – identifying various sources of noise in a system.
3. PCB Layout & Design – component placement, multilayer boards, grounding, shielding and filtering components
4. Practical example of a VGA board design and associated FCC Testing.

REGULATIONS CONTROLLING EMI

The ultimate goal which must be achieved if EMC design is to be considered successful is the attainment of "Agency Certification." A number of international government agencies impose strict criteria on the allowable electromagnetic interference that electronic apparatus can emit. Electronic apparatus is required by law to conform to these agency limits, or else face severe government penalties.

In the United States, the Federal Communications Commission (FCC) is the national regulatory body which sets down strict controls on interference from computing devices. The FCC has divided computer interference into two principal types. The first type, and by far the most demanding of the two, deals with radiated emissions over the frequency range of 30 MHz to 1 GHz. Radiated emissions from personal computers, in a commercial environment, must conform to the limits set out for a Class B computing device pursuant to Subpart J of Part 15 of the FCC Rules. Table I lists the maximum permissible radiation from such devices, measured in terms of Electric Field Strength.

Frequency MHz	Distance Meters	Field Strength* µV/Meter
30–88	3	100
88–216	3	150
216–1000	3	200

Table I. Radiation Limits for Class B Computing Devices According to FCC Rules

The second type of emission deals with interference fed back onto the power lines. The FCC conduction limit on this interference is 250 µV* maximum over the frequency range 450 kHz to 30 MHz. This type of interference is heavily influenced by the design of the switched-mode power supply within the computer cabinet.

FCC Certification is awarded on the submission to the FCC of a complete report which consists of acceptable test results as well as a detailed description of the test and measurement procedure. Testing has to be carried out by an FCC-accredited test laboratory.

Class C Certification, which has less stringent limits, is allowable in certain commercial and industrial applications.

A list of the various international agencies is given in the Reference section. All agencies have very similar requirements to those of the FCC.

NOISE SOURCES

Identification of noise sources or potential noise sources in a system is the first and probably the most valuable step that has to be taken for successful EMI design.

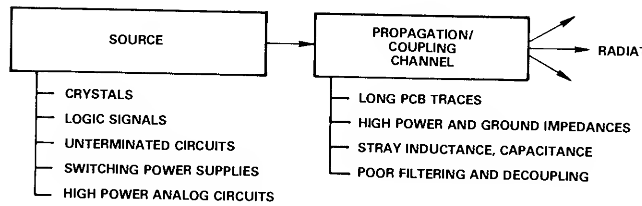


Figure 1. Noise Model of a Video Graphics System

It may even be possible to eliminate a particular noisy circuit completely from the design thus avoiding the later need for filtering. Unfortunately, many possible sources of noise cannot be eliminated from the design, but by being aware of their existence, their effects can be minimized at the source and in the coupling channel by optimum filtering and decoupling. Some of the inherent sources of noise in a video graphics system include:

1. Crystal oscillator and clock frequency division circuits.
2. Circuits with fast transition times (rise/fall times), e.g., logic families that are unnecessarily fast.
3. Unterminated circuits.
4. Stray inductances/capacitances.
5. Switching power supplies.
6. High power analog circuits such as video RAM-DACs.

Crystal Oscillators & Associated Circuitry

A video system usually contains a number of crystal oscillators and associated clock and pixel data circuits, which are required to achieve various on-screen pixel resolutions. In a VGA system, for example, there could be as many as five crystal oscillators varying in frequency from 25 MHz to 65 MHz, and maybe up to 80 MHz. These crystal oscillators and their associated circuitry tend to be rich in unwanted noise and harmonic components. They can be a prime source in the generation of EMI if some basic guidelines are not followed.

*Measured pursuant to §15.840 of the FCC Rules.

Some of the important actions are:

1. Place crystal oscillator circuits as far as possible from analog circuitry and video output connectors.
2. Isolate power supply to crystals through the use of ferrite beads.
3. Avoid the mixing of clock buffers and other logic in the same IC package.
4. Use several low power data drivers or buffers for clock and pixel data lines distributed throughout the board, in preference to using a single high power driver.

With regard to the crystal oscillators themselves, the critical aspects which must be considered include the wave shape and the transition time (rise/fall time). Figure 2 is a plot of the output frequency spectrum of a typical 28.5 MHz crystal oscillator. It shows the amplitude of the harmonic components relative to the fundamental. It can be clearly seen that although the crystal's fundamental frequency lies outside the FCC's lower limit of 30 MHz, for radiated EMI, higher-order harmonic components exist throughout the FCC-controlled band. The frequency of the crystal oscillators should be kept to the required minimum, and transition times should be kept as slow as possible. This reduces the amplitude of unwanted harmonics, while still satisfying system functional performance needs.

The clock circuitry, which includes crystal oscillators and pixel data lines, is the primary source of most of a system's noise. Keeping this circuitry as far and as isolated as possible from other circuitry, especially analog circuitry, is all-important. On the other hand, it could be argued that by running long pixel data and clock lines from such circuitry to the Video RAM-DAC in itself is not desirable. Long lines increase noise coupling to other parts of the system. A tradeoff between length of pixel lines and the placement of high speed clock circuitry must be considered. The designer must attempt to optimize these two competing goals. As was mentioned earlier, the use of multiple low power buffers will help to ease such a conflict. A distance of less that three inches between buffers would be desirable in such circumstances.

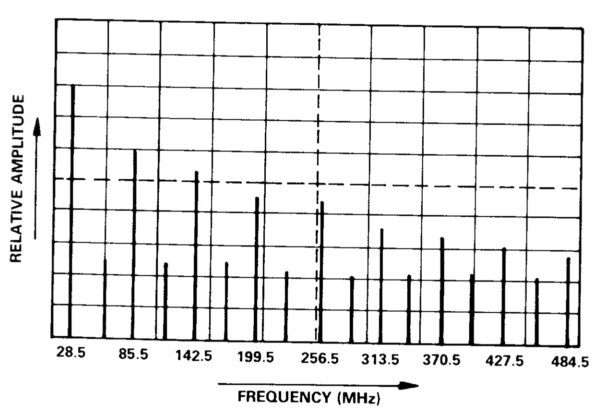


Figure 2. Magnitude of Harmonic Components Relative to the Fundamental for a 28.5 MHz Crystal Oscillator

Other Noise Sources

A number of other noise generators can be easily identified. Circuits with fast transition times including memory chips, logic circuitry and the graphics controller all contribute to the overall noise of the system. The faster the signal transition time, the greater will be the amplitude of the resulting harmonics, as was seen in the previous section relating to crystal oscillator circuits.

As a general rule, devices with the slowest possible rise/fall times that will achieve the system's tasks should be used. Table II lists some typical rise/fall times for various logic families.

Technology	IC Family	Transition Time
TTL	74	10 ns
	74LS	12 ns
	74ALS	3→20 ns
	74S	6 ns
	74AS	2→9 ns
	74F	1.2→8 ns
CMOS	74HC	20→150 ns

Table II. Comparison of Transition Times for IC Logic Families

Stray inductances and capacitances can cause signals to ring, to overshoot or undershoot the steady state voltage levels. This ringing is a source of EMI which can be minimized by keeping wires or traces short and adding series, damping resistances at the source or termination of long signal paths.

Unterminated circuits with floating signal lines should be avoided. Unwanted oscillations can result.

Power to all devices of a system is usually derived from switch-mode power supplies. While the design of the power supply is critical to the reduction of conducted noise in the FCC's band of 450 kHz up to 30 MHz, harmonics generated by the switching power supplies can extend well into the radiation frequency band and thus add to EMI.

Modern high resolution color graphics monitors are driven by analog signal levels direct from the DACs. The relatively high power, analog output levels from the Red, Green and Blue current sources of the video DAC require careful attention. As will be discussed in the PCB layout section, the power to the Video RAM-DAC should be isolated from the remainder of the PCB power plane. If noise on the high speed pixel and clock input section to the Video RAM-DAC has not been minimized, noise will be coupled through to the analog output section and onto the connecting cable to the monitor, causing this cable to act as an antenna. Filtering at the source termination of each of the three DAC outputs can be used if required to minimize the noise further. (See Appendix 1, *Three-Terminal Capacitor.*)

PRINTED CIRCUIT BOARD DESIGN

The extent of radiated emissions from a printed circuit board (PCB), will be determined by the effectiveness of the PCB to act as a propagation channel for unavoidable noise sources, its ability to couple this noise onto other circuitry, and the radiation into free space of this undesired noise. Apart altogether from a PCB's ability to radiate EMI, noise coupled from digital circuits on the board to the video RAM-DAC can adversely affect the system's functional performance.

Causes of EMI

The main sources which conduct or radiate EMI from a printed circuit board are as follows:

1. Common impedance coupling via power and ground traces.
2. Antenna loops formed by ICs and their bypass capacitors. Note that these loops also include the power and ground lead frame members within the IC packages.
3. Printed circuit board traces carrying signal currents. Note again that signal lead frame members within the IC packages are also included.
4. Crosstalk between adjoining signal traces.

Common Impedance Coupling

An example of common impedance coupling via power and ground traces is shown in Figure 3a where a number of logic gates are supplied with power over common printed circuit board traces. A typical V_{IN} input signal to one of these gates is shown in Figure 3b with the resulting transient and signal currents due to the gate switching also shown.

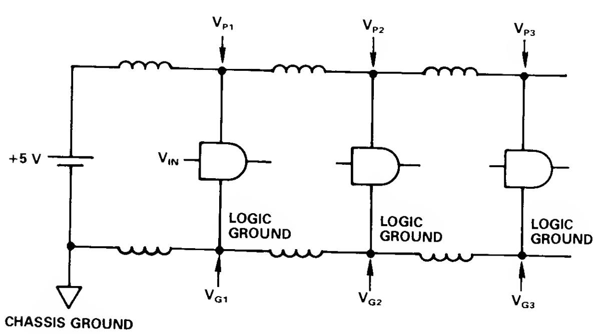


Figure 3a. Common Impedance Coupling via Power and Ground Traces

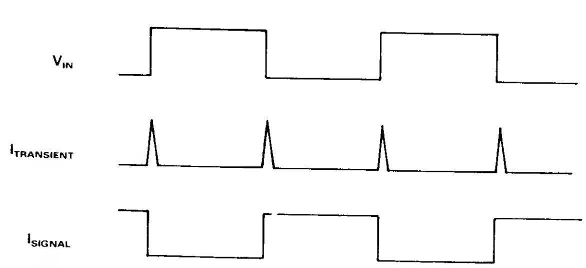


Figure 3b. Signal and Transient Currents Due to Gate Switching

The distributed trace inductances act as impedances to these switching currents spreading the resulting high frequency noise to all nodes common to the culprit. To get an idea of the magnitude of the generated high frequency noise, let's take a look at the effect of a single gate, as shown in Figure 4a. The associated worst signal current for a standard TTL gate is shown in Figure 4b.

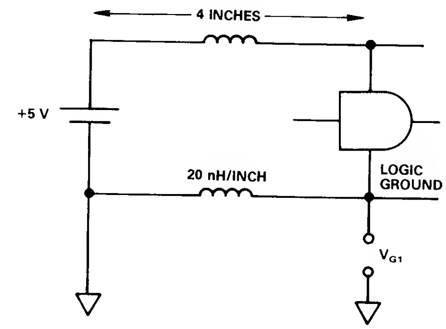


Figure 4a. Common Impedance Coupling Due to One Gate

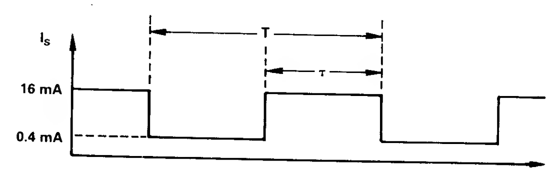


Figure 4b. Signal Current Due to TTL Gate Switching

Consider the harmonic components present in the switching signal current of Figure 4b. This assumes the gate is driving 10 standard TTL loads with a maximum sink current of 16 mA and a maximum source current of 0.4 mA.

With a mark/space ratio of τ/T and using a Fourier Series expansion, the formula for the amplitude of the nth harmonic is given by

$$I_n = \frac{2A\tau}{T}\left[\frac{Sin\left(\frac{n\pi\tau}{T}\right)}{\frac{n\pi\tau}{T}}\right]$$

where n = 1, 2, 3 . . . .

For a square wave τ/T = 0.5, the amplitude of the third harmonic (n=3) is

I_3= 3.4 mA, zero to peak.

At 28.5 MHz, a standard VGA pixel clock frequency, the magnitude of the impedance of the ground trace in Figure 4a is given by

$$Z = [2\pi fL]$$

where f = 28.5 MHz
L = 20 nH/inch (typically)

hence Z = 3.58 Ω/inch.

At 85.5 MHz (3×28.5 MHz) the impedance is 10.74 Ω/inch. Thus the high frequency voltage at the logic

ground node of the switching gate due to the third harmonic alone is equal to

$$V_{G1} = (3.4 \times 10^{-3})(4)(10.74)\ V$$
$$= 146\ mV\ peak\ at\ 85.5\ MHz.$$

This high frequency component and other similar components will be circulated around the printed circuit board via the common ground traces. It will also appear on any cable shielding attached to this common ground trace and, depending on how efficient the cable shield is as an antenna, will be radiated into free space.

Antenna Loops

One of the most important principles of PCB layout and design for noise reduction can be described by the phrase:

"Minimize Signal Loop Areas."

In most circuit designs, we tend to think of the currents we're interested in as flowing "out" of one place, "through" some other place and "to" the target point. Unfortunately however, this often leads us to neglect to consider how these currents will eventually find their way back to their source. Ground and supply voltage points are considered "equivalent," and the fact that they are parts of a network of conductors through which currents flow and develop finite voltages is often not appreciated. These voltages can radiate to cause EMI, see Figure 5.

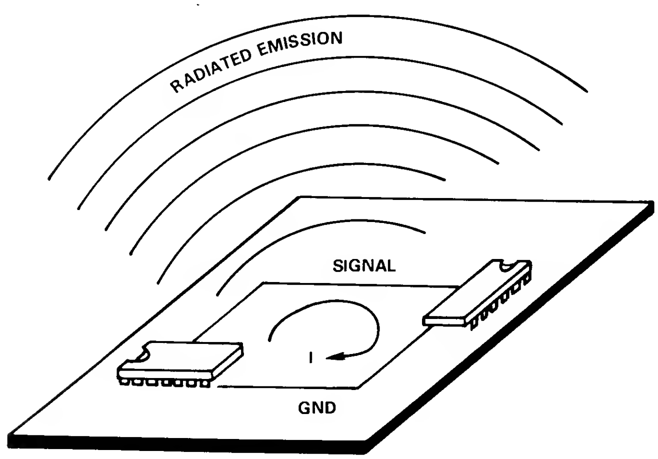


Figure 5. Currents Flowing in Large Loops Add to EMI

Voltages are generated because wires and traces do not have zero impedance due mainly to inherent inductances.

Many of the problems associated with power and ground loops can be avoided through the deployment of effective bypassing techniques.

The aim of effective bypassing is to maximize the charge stored in the bypass loop while simultaneously minimizing the inductance of this loop. Inductance in the loop acts as an impedance to high frequency transients and results in power supply spiking. Figure 6a shows a poor bypass arrangement and the associated inductances due to the large loop area are illustrated in Figure 6b.

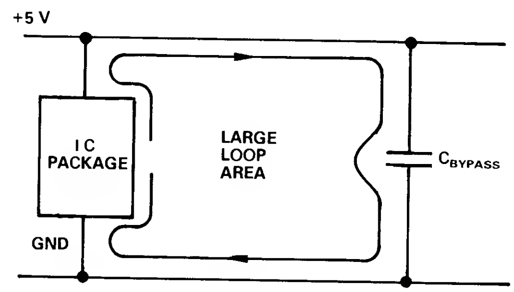


Figure 6a. Large Loop Associated with Poorly Placed Bypass Capacitor

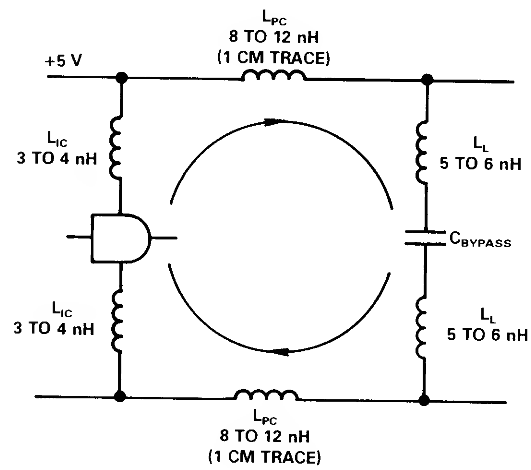


Figure 6b. Equivalent Circuit of Bypass Loop of Figure 6a

where L_L = inductance of the lead from the capacitor body to the PC board

L_{PC} = inductance of the trace between the lead arrival on the PC board and the IC pin

L_{IC} = inductance of the lead frame member carrying power within the IC package.

As well as loop inductances due to the above, the series inductance of the bypass capacitor itself must also be considered. It is well known that there is more inside a capacitor's body than a pure capacitance.

The simplified equivalent circuit of a 0.1 μF capacitor in Figure 7 shows an effective series resistance (ESR) and effective series inductance (ESL) in series with the ideal 0.1 μF capacitance.

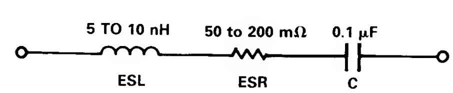


Figure 7. Equivalent Series Representation of a Bypass Capacitor

Figure 8 shows the complete inductive loop associated with the bypass circuit.

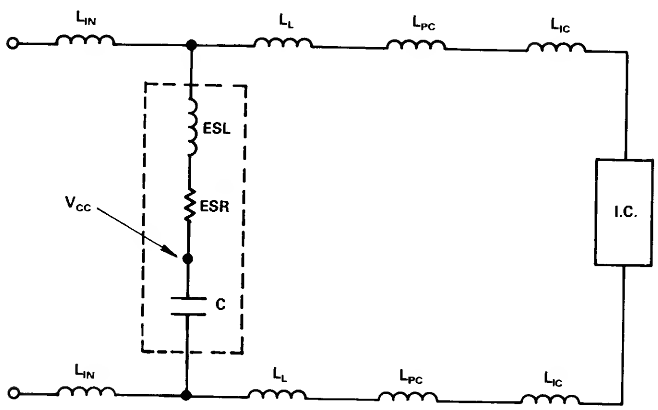


Figure 8. Inductive Loop of a Bypass Circuit

These inductances increase the total series inductance of the bypass loop and hence lower the series resonant frequency as determined by the equation:

$$fo = \frac{1}{2\pi\sqrt{LC}.}$$

Above the series resonant frequency the impedance becomes more inductive, increasing linearly with increasing frequency. For instance, a 0.1 μF ceramic radial lead capacitor with 1/4 inch leads generally resonates around 10 MHz.

The minimum value of bypass capacitor required is determined by the maximum amount of voltage drop allowable across the capacitor as a result of the transient current. An approximate value for a bypass capacitor is given as

$$C = \frac{I.\Delta t}{\Delta V} \; Farads$$

where I = Maximum Transient Current
Δt = Transient Duration
ΔV = Allowable Voltage Drop.

For example, a typical 74 HC I_{CC} transient is 20 mA high lasting 20 ns. If the voltage drop is to be kept below 100 mV, then the required bypass capacitor is

(20 mA) (20 ns) / (100 mV)

or 4 nF per output.

However, any series inductance in the bypass loop will cause additional voltage spiking. For any given magnitude of noise spike, an approximate expression for the maximum amount of series inductance is given by

$$L = \frac{V.\Delta t}{\Delta I} \quad Henrys$$

where V = Maximum Noise Spike
Δt = Transient Duration
ΔI = Transient Current.

The typical 74 HC I_{CC} transient of 20 mA has a rise/fall time of 4 ns. If we wish to restrict the inductive noise spike to, say, 100 mV peak, the maximum amount of series inductance is

(100 mV) (4 ns) / (20 mA)

or 20 nH.

Referring back to Figure 8, this means that the combined total of ESL, L_L, L_{PC} and L_{IC} must be kept below 20 nH. To a greater or lesser extent the first three terms are within the PC board designer's influence; the fourth term, the inductance of the IC lead frame member or L_{IC}, is invariable, being determined by the IC package. The use of PLCC packaged parts, such as the ADV478/ADV471, inherently reduces L_{IC} to 2–3 nH as against 10–12 nH for the more traditional DIP parts (see section on "Surface Mount Technology").

Appendix 1 examines in greater detail the characteristics and filtering capabilities of various bypass elements including two and three terminal capacitors.

Multilayer PC Boards

In the design of a high performance, high speed graphics system, it is recommended that a four-layer printed circuit board be used.

Figure 9 shows a cross-sectional view of a four-layer printed circuit board, with power and ground planes separating the signal-carrying traces of the component and solder sides of the PCB. As well as using multilayer boards, consideration should be given to the relevant placement of components. Figure 10 shows a suggested component placement scheme.

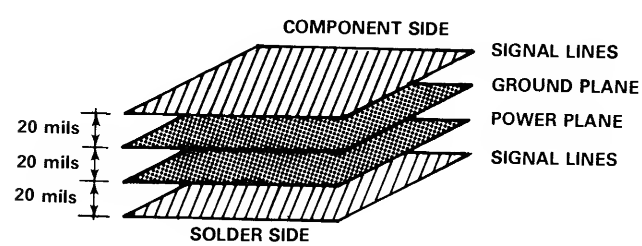


Figure 9. Four-Layer Printed Circuit Board Construction

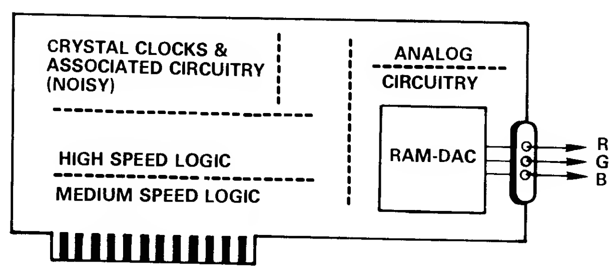


Figure 10. Printed Circuit Board Component Placement

Power and Ground Planes

Power supply decoupling attempts to contain the transient currents within the bypass loop. However it cannot be 100% successful, and some high frequency components will escape onto the power and ground traces. High frequency signal currents will also be flowing in the power and ground traces. In order to avoid common-impedance noise coupling due to these currents, it is necessary to reduce the impedance of the power and ground traces to an absolute minimum. The only satisfactory way to achieve this is not to use traces at all but to use power and ground planes. On a PC-card-sized, two-layer board with one side devoted to a ground plane, the impedance of the plane is in the tens of milliohms range.

A four-layer board allows another plane to be used as a power plane. Low impedance power and ground contacts are thus available over the full area of the board. Additionally, in a four-layer board with power and ground planes inside the board and signal traces on the top and bottom of the "sandwich," overlapping power and ground planes act as an inherent distributed capacitor, as shown in Figure 9. This provides some measure of high frequency decoupling. From the signal interconnect point of view, the major advantage of using a ground plane is the very substantial reduction in signal loop area it provides. In a typical PCB layout, signal current flows out through one trace and back through a ground trace. Such a path can include a large loop area; a large loop area, as has already been discussed, implies high inductance for the traces with follow-on consequences of signal ringing, EMI radiation and crosstalk. To reduce the inductance it is necessary to reduce the loop area through which the signal current flows. The use of power and ground planes minimizes loop areas, thereby reducing inductances and resulting EMI.

The electromagnetic fields associated with an idealized case of two parallel wires carrying equal and opposite currents are shown in Figure 11.

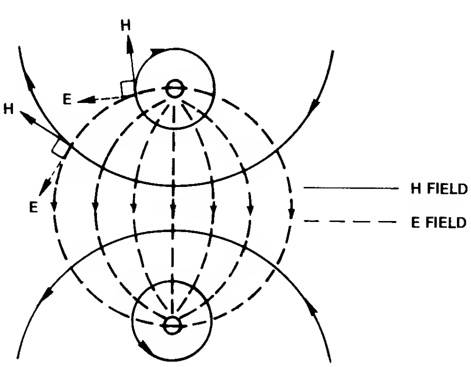


Figure 11. Electromagnetic Field about Two Parallel Conductors Carrying Equal and Opposite Currents

The two fields (electric, E, and magnetic, H) tend to be confined between or near the conductors. The electric field is strongest in the plane of the conductors. The magnetic field is nonzero at points close to the conductors, but farther away (relative to the wire spacing) the fields from both conductors tend to cancel out. Keeping the conductors together promotes field cancellation which can be viewed either as minimizing the loop area or minimizing the inductance; the results are the same.

Introducing a ground plane (sheet of copper) halfway between the wires, as shown in Figure 12, does not disturb the field pattern even when the lower wire is removed.

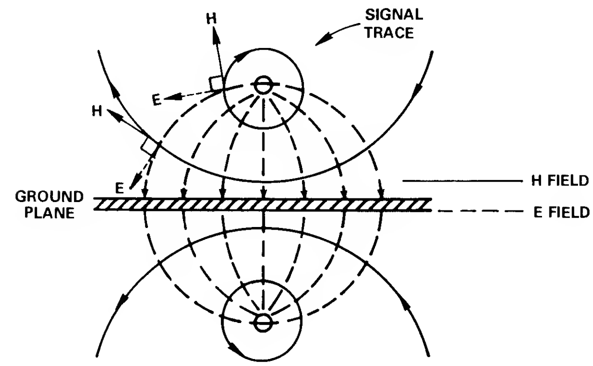


Figure 12. Electromagnetic Field about Two Parallel Conductors Separated by a Ground (Copper) Plane

A virtual image of the lower wire has been produced in the copper plane maintaining the original field configuration. This is the basis of microstrip. With a properly designed ground plane system, the return current will always flow under the signal trace, the path of lowest impedance.

Digital Signal Interconnections

The use of a ground plane allows the signal interconnects to be viewed as microstrip transmission lines whose characteristic impedances, propagation delays, etc., can be readily calculated. Microstrip is the name given to a transmission line which consists of a signal trace separated from a ground plane by a dielectric. Figure 13 shows the cross section of such a line.

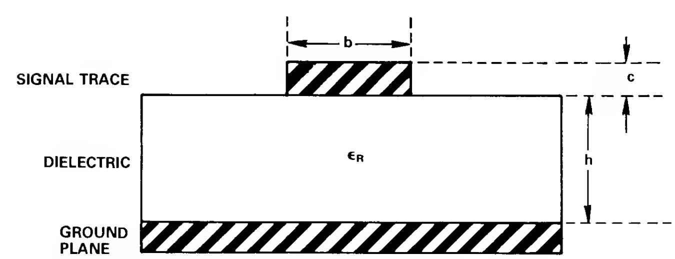


Figure 13. Cross Section of Microstrip Transmission Line

The characteristic impedance, Z_O, of this line is

$$Z_O = \frac{87}{\sqrt{\epsilon_R + 1.41}} Ln \left\{ \frac{5.98\,h}{0.89\,b + c} \right\} \Omega$$

where ϵ_R = Relative Dielectric Constant of Board

typically ϵ_R = 5 for glass/epoxy boards.

b, c, h = dimensions indicated in Figure 13

The propagation delay, t_{PD}, of a microstrip line is given by

$$t_{PD} = 1.017 \sqrt{0.475\, \epsilon_R + 0.67}\ ns/ft.$$

Note that this propagation delay is dependent only on the dielectric constant and not on the line geometry.

The graph below shows impedance values for various configurations of microstrip line.

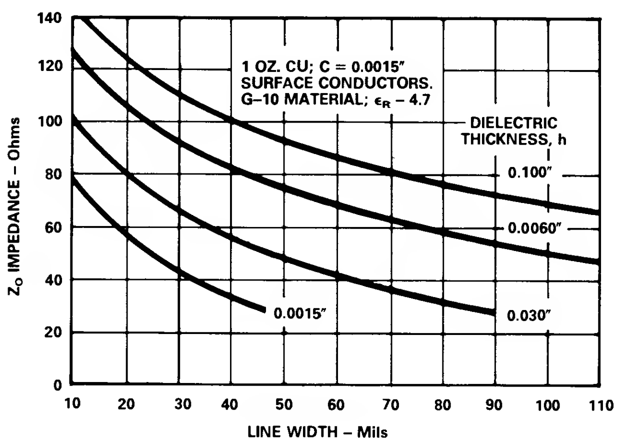


Figure 14. Impedance Versus Line Width & Dielectric Thickness for Microstrip Lines

Gross impedance mismatches between the transmission line's characteristic impedance and the source (driver output) or load (receiver input) impedances connected to the line reflect the signal back and forth on the line. These reflections will cause overshoot, EMI radiation and crosstalk. By properly terminating the line with either source or load impedances which match that of the transmission line, reflections can be eliminated or substantially reduced. However, not every signal interconnect demands line termination; the need is determined by the relationship between the rise (or fall) time of the signal and the time required for the signal to travel the length of the interconnect. As a general guideline for digital signals, line termination is needed if the one way propagation delay, t_P, over the length of the interconnect is greater than one eighth of the signal rise time, t_R, i.e., line termination is needed if

$$t_P \geq (1/8) \bullet t_R\ secs.$$

A number of dc and ac termination techniques exist which trade increased power dissipation against component count. The simplest termination technique which dissipates no extra power is a series termination one where a resistor is placed in series with the signal interconnect at the source end of the line, see Figure 15. The resistor should have a value equal to the characteristic impedance of the line minus the output impedance of the driver and should be of metal-film construction or some other low-inductance material. The load impedance is considered an open circuit. Series termination is most suitable for systems where only one receiver (e.g., ADV478/ADV471) is connected to the line. Note that if pull-up resistors are required on digital or clock signals, they should be connected to the PCB Power Plane (V_{CC}).

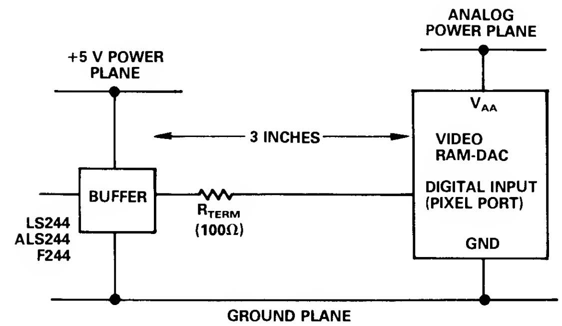


Figure 15. Series Termination of Signal Lines

Crosstalk

Crosstalk is any unwanted signal coupling between parallel PC-board traces due to mutual inductance (L_M) and capacitance (C_M), as illustrated in Figure 16.

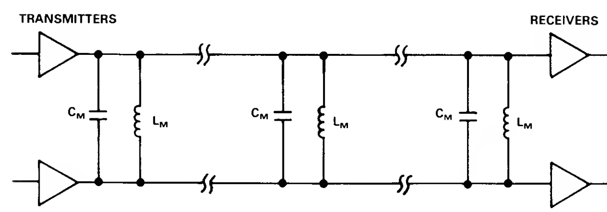


Figure 16. Capacitive and Inductive Coupling between Signal Traces

In general, crosstalk is directly proportional to line impedances, frequency and line lengths and inversely proportional to line spacing. Much of the induced crosstalk in a signal line is from immediately adjacent transmission lines which suggests that wider spacing between lines will reduce the problem. This may not always be possible in closely spaced circuits, so an alternative approach is to shield the signal lines by inserting narrow grounded traces between each signal line on the same wiring plane, as shown in Figure 17.

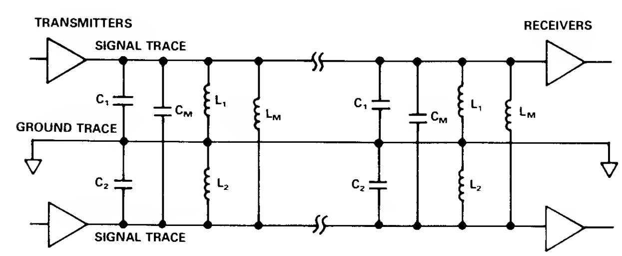


Figure 17. Ground Trace between Signal Lines Reduces Crosstalk

At high frequencies capacitive coupling dominates. The addition of a shield (or ground trace) between the signal lines changes the equivalent circuit. Crosstalk is now reduced since the inductance L_M is now much larger than either L_1 or L_2 and capacitance C_M is much smaller than either C_1 or C_2.

Separate Power Plane for Video RAM-DAC

To further isolate the Video RAM-DAC from the PCB's power supply, V_{CC}, it is recommended that a separate power plane, V_{AA}, be used for the video RAM-DAC and its associated circuitry. This analog power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a suitable filtering device such as a ferrite bead (see Appendix 1 *—Ferrite Bead Inductor*). This ferrite bead should be located no more than three inches away from the Video RAM-DAC. In the case of Analog Devices' ADV478 and ADV471, which have multiple power (V_{AA}) pins, it is important to connect all these V_{AA} pins to the analog power plane. This eliminates any possibility of latchup in the device.

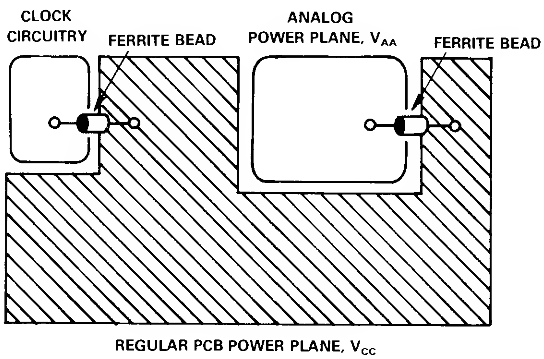


Figure 18. Power Plane Decoupling Using Ferrite Beads

Common Ground Plane

Due to the presence of RAM on board the ADV478/ADV471 and ADV476, it is not recommended to isolate the device's ground circuitry from the main PCB ground. Corruption of data could occur. These Video RAM-DACs should have all GND pins connected to the PCB's regular ground plane.

Analog Outputs

The analog outputs of Analog Devices' video RAM-DACs are driven by switched current sources. These parts are designed to drive either a singly or doubly terminated 75 Ω load. The doubly terminated configuration shown in Figure 19 is the preferred choice.

DAC output traces on a PCB should be treated as transmission lines. It is recommended that the Video RAM-DAC be placed as close as possible to the output connector, with the analog output traces being as short as possible (less than 3 inches). The 75 Ω termination resistors should be placed as close as possible to the DAC outputs and should overlay the PCB's ground plane.

As well as minimizing reflections, short analog output traces will reduce noise pick up due to neighboring digital circuitry.

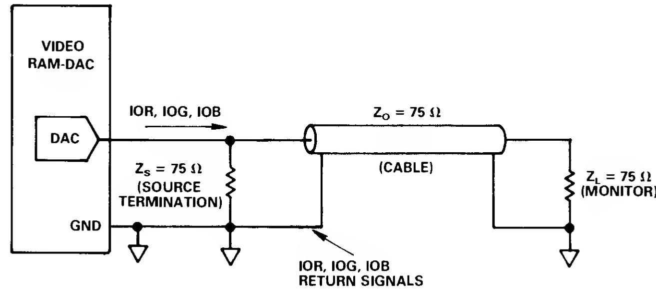


Figure 19. Recommended Analog Output Termination for Video RAM-DACs

Surface Mount Technology (SMT)

Surface mount technology (SMT) offers many EMI advantages over traditional through-hole designs. Because SMT allows the designer to place components on both sides of the printed circuit board as well as featuring smaller component sizes, it provides superior PCB integration. This means that loop lengths can be reduced and noisy signal traces can be shortened, all having a positive effect on EMI. The shorter lead lengths of SMT packages decrease inductance, thereby providing better high frequency performance.

Many, if not all components required for a video graphics system are available as surface mount devices. Memories, controller chips and logic are all available in small SMT packages. Resistors and capacitors can also be purchased in a small "chip" format.

As well as producing Video RAM-DACs in a dual-in-line package (DIP), e.g., the ADV476 (28-pin DIP), Analog Devices packages its ADV478/ADV471 in 44-pin plastic leaded chip carriers (PLCC). This package has substantial advantages over DIP packages in that the lead-frame inductance is small (2-3 nH) and constant for any pin around the package. A DIP package usually has power and ground on diagonally opposing corner pins which presents a much larger lead-frame inductance (10–12 nH). Additionally lead-frame inductance varies with pin position.

In addition to the PLCC package the ADV478/ADV471 video DACs have a number of design features intended to minimize EMI problems.

The pinout of the ADV478/ADV471 in Figure 20 shows four power pins and two ground pins. In operation, the four V_{AA} pins are tied together at the package and supplied with a single +5 V supply. Similarly the two ground pins are tied together at the package and connected to the PCB ground. Internally, however, power rail routing has been separated according to functionality. The various V_{AA} pins are used to drive different internal sections of the ADV478/ADV471. One V_{AA} pin provides a common power rail for "digital" logic;

another provides an "analog" power rail for the DAC and reference circuitry; while yet another provides power to the n-substrate of the device. Since all p-channel transistors have as their back-gate the n-substrate, a separate substrate supply acts to isolate the DAC power rail from noise transients injected into the substrate by switching transistors. The use of multiple power and ground pins results in reduced voltage spiking and improved power supply rejection at the DAC outputs.

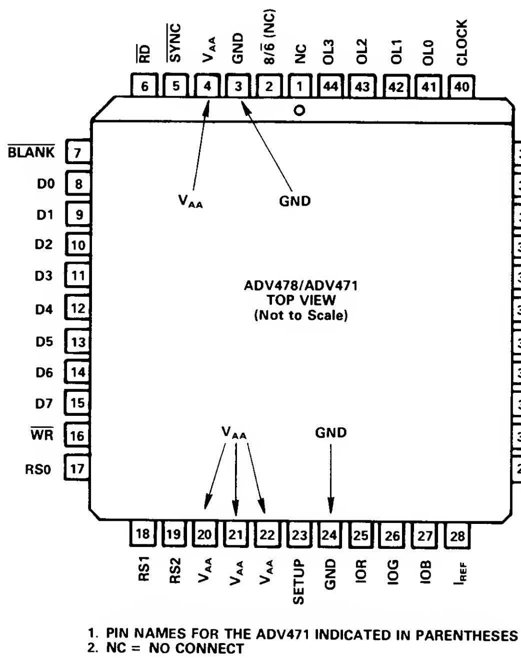
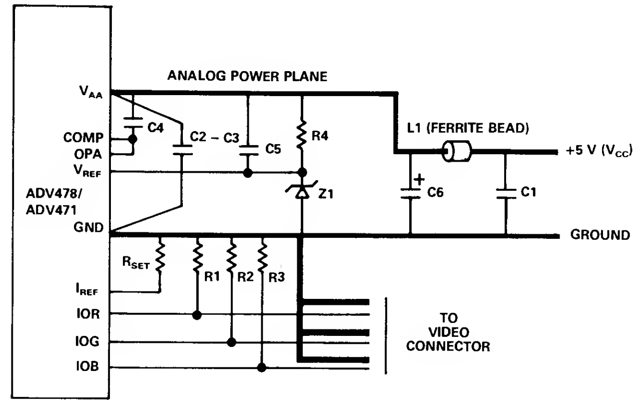


Figure 20. ADV478/ADV471 PLCC Pin Assignment Showing Multiple Power and Ground Connection Points

CIRCUIT LAYOUT FOR THE ADV478/ADV471

A recommended layout and component listing for the ADV478/ADV471 is shown in Figure 21. More details regarding the characteristics of various decoupling and filtering components can be found in Appendix 1 of this application note.



COMPONENT	DESCRIPTION	VENDOR PART NUMBER
C1 – C5	0.1 μF CERAMIC CAPACITOR	ERIE RPE112Z5U104M50V
C6	10 μF TANTALUM CAPACITOR	MALLORY CSR13G106KM
L1	FERRITE BEAD	FAIR-RITE 2743001111
R1, R2, R3	75 Ω 1% METAL FILM RESISTOR	DALE CMF-55C
R4	1 kΩ 5% RESISTOR	
R_{SET}	1% METAL FILM RESISTOR	
Z1	1.235 V VOLTAGE REFERENCE	ANALOG DEVICES AD589KH

Figure 21. Connection Diagram and Component Listing for the ADV478/ADV471

GETTING FCC CERTIFICATION

The final chapter in EMI design is the actual test. With good design practice and even a partial adherence to some of the issues raised in this application note, no difficulty should be encountered in achieving certification. The testing itself however must be carried out with great care in order to do justice to your design. It should be remembered that in the case of a peripheral device such as a VGA board, FCC testing is applied to a complete operating computer system. This complete system must pass with the VGA board present before the VGA board itself is considered to have passed.

A complete operating computer system is configured using the following:

1. a PC compatible computer with keyboard
2. a printer connected to the printer port
3. a mouse or modem connected to the serial port
4. a monitor.

The PC and all its peripherals must be operating when measurements are made.

It is paramount that only the best equipment is used. If for example a noisy monitor is used, the test results might not pass the agency limits, not because your board is at fault, but perhaps because of a poor quality, noisy monitor used in the test. An excellent choice of monitor is IBM's 851X series. Another principal culprit, causing EMI in such a system, is the parallel printer cable. A good quality, shielded cable must be used.

If you are using an outside test house, it is advisable to be present during testing, or at least have a representative from your company who understands the operation of the system and its various components.

AD/VGA

Analog Devices has designed its own high performance graphics board, AD/VGA for evaluation purposes. The board design is based on the ET3000AX* Video Graphics Controller from Tseng Labs and the high performance ADV478/ADV471 Color Palette RAM-DAC from Analog Devices. The board is fully compatible with all IBM PC† video standards as well as IBM PS/2† Video Graphics Array (VGA). It has additional modes including 800 × 600 resolution with 256 colors as well as 1024 × 768 in 16 colors. These modes require pixel data rates of up to 45 MHz or 66 MHz. The silkscreen showing component placement and type for the AD/VGA board is shown in the appendix.

The board has been certified to comply with the limits for a Class B computing device pursuant to Subpart J of Part 15 of FCC Rules.

FCC ID: HRF55L8826VGA

One actual set of measurements for radiated emissions from the AD/VGA board is shown in Appendix 2. Results can be compared to the FCC limits as listed in Table I.

The AD/VGA board was installed in a DELL SYS 200‡ computer using an IBM 8514 monitor. A modem, printer and mouse were attached. These measurements were made in 132 × 44 text mode.

A complete set of test results is available for inspection.

REFERENCES

1. International EMI Emission Regulations

USA:	FCC–15 Part J
West Germany:	VDE 0871/VDE 0875
Canada:	CSA C108.8–M1983
Japan:	CISPR(VCCI)/PUB 22

2. EMI Countermeasures – Application Guidance – Murata Mfg. Co. Ltd.
3. Henry. W. Ott, "Noise Reduction Techniques in Electronic Systems." John Wiley, N.Y., 1986.
4. Paul A. Brokaw, "An I.C. Amplifier Users' Guide to Decoupling, Grounding and Making Things Go Right for a Change." Analog Devices Data-Acquisition Databook 1984, Volume 1, Pages 20–13 to 20–20.
5. Motorola Inc., "MECL Design Handbook" 2nd Edition, 1972.

†IBM PC, IBM PS/2, IBM8514/A and VGA are trademarks of International Business Machines Corp.
‡DELL SYS 200 is a trademark of Dell Computer Corporation.
*ET3000AX is a trademark of Tseng Laboratories, Inc.

APPENDIX 1

EMI FILTERING COMPONENTS

No matter how well a PCB is laid out, there will always be a need for some kind of filtering. This section of the application note examines, in some detail, a number of filtering devices which are suitable for a high speed graphics system. The frequency characteristics of such devices as well as their inherent limitations will be discussed.

The effect of an EMI filter is generally expressed in terms of insertion loss. Noise suppression is described as a logarithm of the ratio of the output voltage without a filter to that with a filter in the circuit and is normally expressed in units of dBs. The simplest example is a first order device, a parallel capacitor or series inductor. A first order filter has an insertion loss slope of 20 dB per decade.

Table 1-1 shows a list of suitable filtering devices and their useful frequency bandwidth.

Filtering Device	Effective Bandwidth
Two-Terminal Capacitor	100 kHz–50 MHz
Ferrite-Bead Inductor	10 MHz–500 MHz
Three-Terminal Capacitor	1 MHz–800 MHz
Four-Terminal LC Filter	100 kHz–1 GHz

Table 1-1. Effective Bandwidth of Various Filtering Devices

The favorite and most widely used filtering device in electronic apparatus today is undoubtedly the "Bypass-Capacitor." It is simple to use, very effective and cheap. Unfortunately though, its effect in a high frequency graphics systems is sometimes the opposite to what is desired. A little thought regarding choice of capacitor, in terms of construction and value can lead to a dramatic improvement in noise performance.

Two-Terminal Capacitor

Let us first take a more detailed look at the structure of a real capacitor.

The impedance of an ideal capacitor connected between line (V_{CC}) and ground is given by

$$Z_C = \frac{1}{2\pi f C.}$$

From Figure 1-1, we can see that the insertion loss of an ideal capacitor increases with frequency at a rate equal to 20 dB/decade. In other words, the capacitor's filtering effect is greatest for higher value frequency components. Increasing the value of capacitance has the effect of filtering out lower frequency components. In the real world, however, a two-terminal capacitor has inductance in series with the capacitance, due to the inherent inductance of the lead wires as shown in Figure 1-2. The reactance characteristic of such a capacitor is shown in Figure 1-3 with the composite insertion loss characteristic shown in Figure 1-4. Clearly, the inductance, ESL, limits the insertion loss. The residual inductance of a capacitor is a function of both the electrode construction as well as lead length. This inductance can vary between 5 nH and 150 nH.

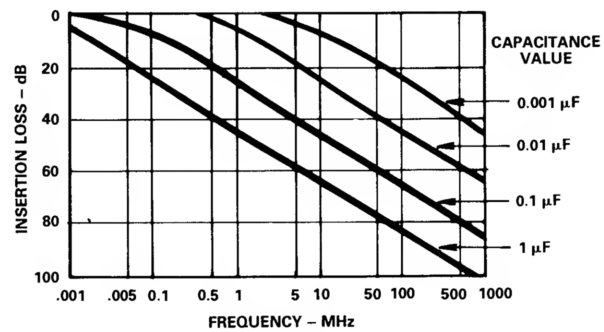


Figure 1-1. Insertion Loss Versus Frequency for Ideal Capacitors

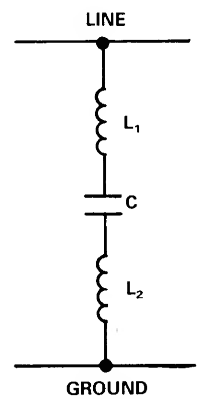


Figure 1-2. Real Capacitor Showing ESL Due to L_1 and L_2

Table 1-2 shows typical values of series inductance for various capacitor types.

Capacitor Type	Capacitance µF	Equivalent Series Inductance (ESL) nH
Lead Type		
Monolithic Ceramic	0.01	5
	0.1	5
	1.0	6
Disc/Lead Type Ceramic	0.0002	4.5
PolyethyleneTelephthalate	0.03	9
Mica	0.01	52
Polystyrene Film	0.001	12
	0.1	100
Tantalum Electrolytic (with Solid Electrolyte)	16	5
Aluminum Electrolytic		
RF Specific	470	13
Standard	470	130

Table 1-2. ESL for Various Capacitor Constructions and Values

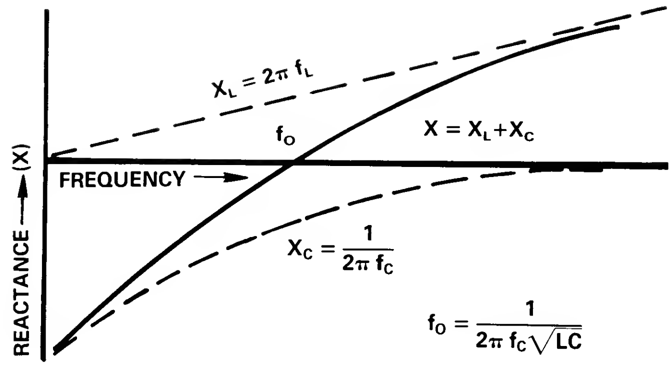


Figure 1-3. Reactance Characteristic of a Capacitor with Finite ESL

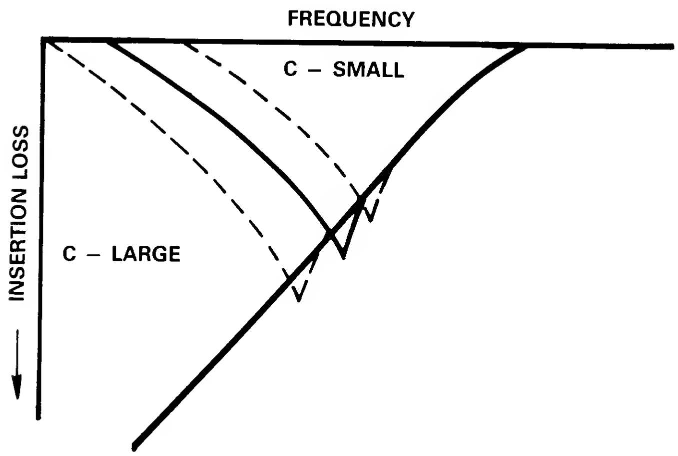


Figure 1-5. A Large Value Capacitor Has a Decreased f_O

The resulting effect of this equivalent series inductance (ESL) is a reduction in the effectiveness of the capacitor at filtering frequency components beyond a certain point, known as the resonant frequency, f_O. It can be seen from Figures 1-4 to 1-6 that increasing the capacitance value can have the effect of reducing the resonant frequency thereby reducing the ability of this device to filter out higher frequency components. It is therefore imperative that a capacitor with low residual inductance be used. A good choice of high frequency decoupling capacitor would be a 0.1 μF lead type monolithic ceramic capacitor (MCC). This has a series inductance of approximately 5 nH. The resonant frequency, f_O, is thus kept high thereby maximizing high frequency rejection.

As well as series inductance, a capacitor will also contain resistance, referred to as equivalent series resistance (ESR). See Figure 1-7.

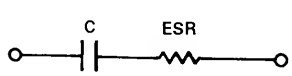


Figure 1-7. Real Capacitor showing ESR

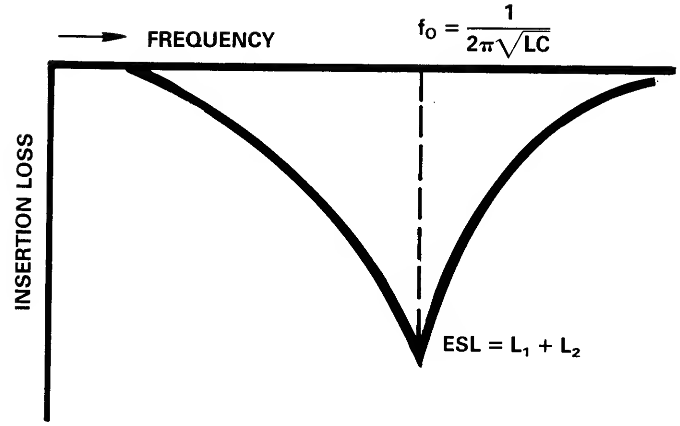


Figure 1-4. Insertion Loss of a Capacitor is Limited by f_O

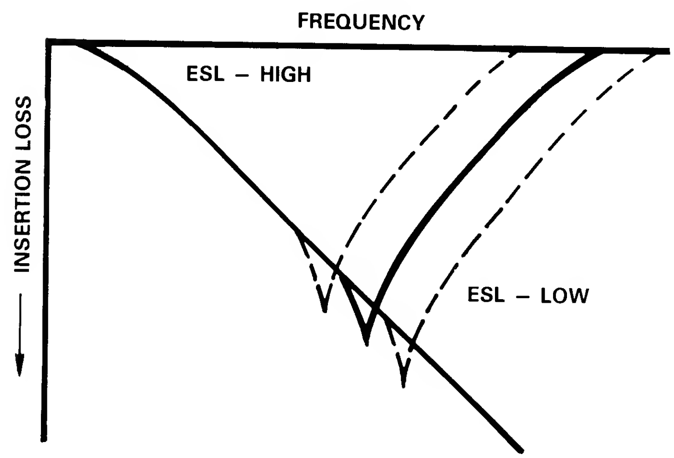


Figure 1-6. A Capacitor with Low ESL Has an Increased f_O

This resistance imposes a finite limit on the ability of a capacitor to bypass high frequencies to ground. Total impedance of the device can never be lower than that imposed by the equivalent series resistance. A capacitor having a high ESR will exhibit a flattened insertion loss curve, compared with the sharp resonant point typically observed in capacitors with lower ESR values.

The overall equivalent circuit of a two-terminal capacitor with ESL and ESR is shown in Figure 1-8.

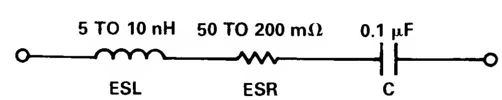


Figure 1-8. Equivalent Circuit of a Real Capacitor

Maximum noise reduction will be achieved through the selection of capacitors with lowest ESL and ESR values.

At least one decoupling capacitor should be used for each IC in the system. In the case of the Video RAM-DAC, it is recommended that for high frequency suppression, a 0.1 μF ceramic capacitor be used to decouple

each group of V_{AA} pins to ground. Low frequency components can be decoupled through the use of a 10 μF tantalum capacitor. Figure 21 shows the recommended decoupling scheme for the ADV478/ADV471. Capacitors with minimal lead length, should be placed as close as is physically possible to the device.

Three-Terminal Capacitor

Three-terminal capacitors have filtering characteristics extending to several hundred MHz. Two leads at the line side of the capacitor provide line input and output respectively, see Figure 1-9. This reduces effective series inductance.

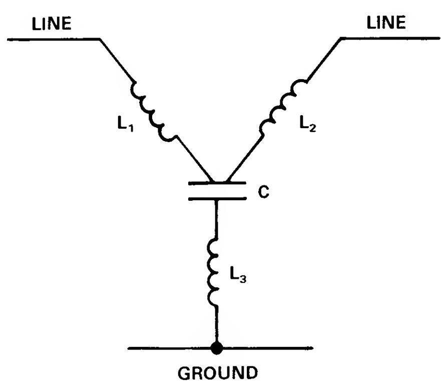


Figure 1-9. Equivalent Circuit of a Three-Terminal Capacitor

One particular example of the use of such a three-terminal device would be at the analog outputs of the Video RAM-DAC. The NFV510 series of three-terminal capacitors from Murata have a sharp insertion loss characteristic. This means that high frequency signals can be filtered without affecting the integrity of the signal itself. The NFV510 series has an excellent shape factor, due to an inherent roll-off of 100 dB/decade, see Figure 1-10. It therefore suppresses noise without reducing resolution. In the case of a graphics system with video output rates of 80 MHz, the NFV510-655 T2A 107 could be employed at the outputs of each of the red, green and blue DACs.

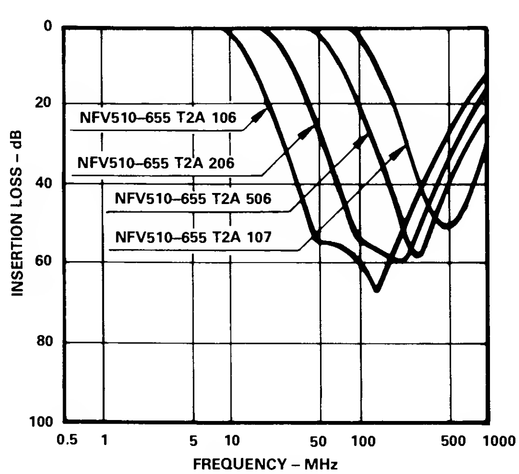


Figure 1-10. Frequency Response of the NVF510 Series of Three-Terminal Capacitors

Ferrite Bead Inductor

A ferrite is another very useful component in the effective suppression of EMI. One can consider a ferrite bead as a high frequency resistor with no resistance at dc. Ferrites have filtering characteristics which extend well into the megahertz range. They can be used to provide isolated power planes, e.g., a PCB's power plane may be subdivided into an analog power plane (V_{AA}) and clock circuitry power plane, see Figure 18. Ferrite beads work both ways; one prevents noise components on the PCB power plane from being coupled onto the analog power plane, while the other filters out noise components from the clock circuitry. The analog power plane provides power to the Video RAM-DAC and all its associated analog circuit, while the clock circuitry power plane provides power to the crystal oscillators and clock divide circuitry.

It is not, however, recommended to use a ferrite bead in separating ground planes; a separate analog ground plane to the Video RAM-DAC may have disastrous effects on the contents of the on-board color look-up table. One common ground plane should encompass the entire PCB.

The system's shield ground or earth may be connected through a ferrite bead to the regular PCB ground.

Ferrite is the generic term given to a class of non-conductive ceramics. They are constructed using combinations including oxides of iron, cobalt, nickel, zinc, magnesium and some rare earth materials. It is important to be careful in choosing ferrite beads. Ferrite composition and therefore filtering characteristics can vary quite significantly from manufacturer to manufacturer. Analog Devices recommends the use of the BL01/02/03 series of ferrite bead inductors from Murata as well as the Fair-Rite 2743001111. The frequency characteristic of a radial single bead ferrite bead is shown in Figure 1-11.

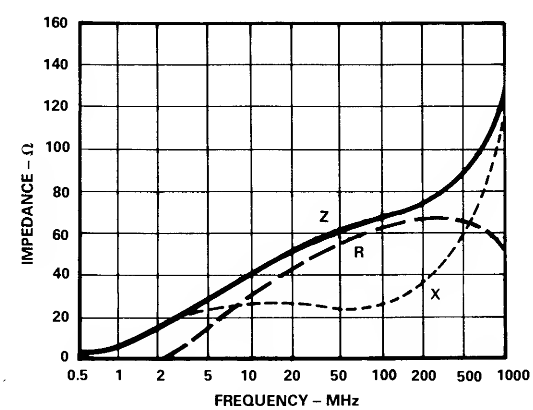


Figure 1-11. Frequency Characteristic of the BL01RN Ferrite Bead Inductor

DC Power Filter

In some cases it might be necessary to filter the power source's high frequency components. This is often the case when switched mode power supplies are used. If it is found that the system's power supply is excessively noisy, one could consider the use of a dc power filter

such as a BNX002-01 from Murata or equivalent. This filter which consists of a large value monolithic 4-terminal capacitor, a feed-through capacitor and beads, as shown in Figure 1-12, produces an effective filtering effect, 40 dB min over the frequency range 1 MHz to 1 GHz. Figure 1-13 shows the filtering characteristic of the BNX series of power filters from Murata.

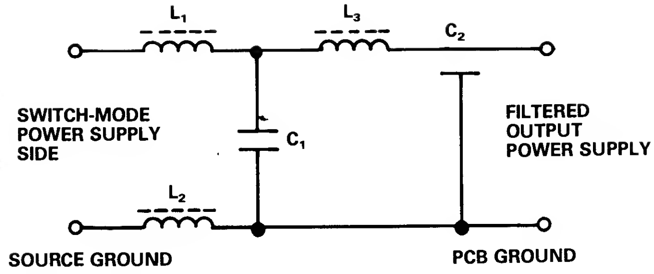


Figure 1-12. Equivalent Circuit of a dc Power Filter

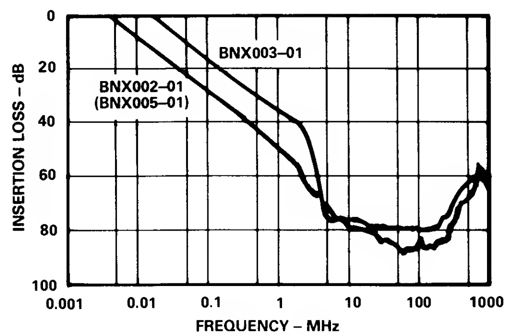


Figure 1-13. Frequency Response of the BNX Series of dc Power Filters

APPENDIX 2

FCC TEST RESULTS OF AD/VGA

Frequency	EUT Orientation	Ambient Radiation	Antenna		EUT Radiation			Field Strength
			Polarization	Height	Factor	Maximum	Corrected	
MHz	Degrees	dB μV	H/V	Meters	dB/M	dB μV	dB μV/M	μV/m
37.2	60	6.7	V	1	12.9	18.8	31.7	38.5
48.1	20	3.6	V	1	12.9	19.0	31.9	39.5
60.6	90	7.8	V	1	11.4	20.3	31.7	38.5
62.8	90	9.8	V	1	10.6	17.3	27.9	24.8
69.5	50	8.6	V	1	8.9	19.9	28.8	27.5
70.9	30	10.8	V	1.5	8.9	24.0	32.9	44.2
72.7	90	10.9	V	1	8.6	20.1	28.7	27.2
75.8	30	14.2	V	1	8.4	22.4	30.8	34.7
78.9	30	13.1	V	1	8.4	24.5	32.9	44.2
80.7	0	10.9	V	1	8.5	19.1	27.6	24.0
88.0	0	12.0	V	1.5	10.0	22.1	32.1	40.3
119.7	330	4.4	H	1.5	15.8	16.9	32.7	43.2

Sample of FCC Test Results for AD/VGA Board

APPENDIX 3

AD/VGA COMPONENT PLACEMENT (SILKSCREEN)